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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
TSAI, HENRY	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/802,289	Applicant(s) SAULSBURY ET AL.	
	Examiner Henry W.H. Tsai	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/31/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5-8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b). Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1, 7, 11, 13, 14, 17, and 18 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 19, and 24-27 of copending Application No. 09/802,120. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 19, and 24-27 of copending Application No. 09/802,120 contain(s) every element of claims 1, 7, 11, 13, 14, 17, and 18 of the instant Application and as such anticipate(s) claims 1, 7, 11, 13, 14, 17, and 18 of the instant Application

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). "
ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).
This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claims 2 and 12, "every two of said N2 number of processing paths share one of said plurality of register files" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: "S0"; "S1"; and "S2" (in Fig. 3). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following

reference sign(s) mentioned in the description: "200" (Page 20, line 21). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to because:

at page 10, lines 32-33, "the VLIW instruction word passes to execute stages 130 via 118" is not shown in the drawings; and in Fig. 3, "Trac Stage" should read -Trap Stage-.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

7. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and

legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

8. The abstract of the disclosure is objected to because the abstract exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

9. The disclosure is objected to because of the following informalities:

at page 13, line 32, "20" should read -2^0-; and "220" should read -2^{20}-; and

at page 14, line 4, "220" should read -2^{20}-.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1, 3, 5, 6, 8-11, 13, 15-17, 19, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Drabenstott et al. (U.S. Patent No. 6,366,999), hereafter referred to as Drabenstott et al.

Referring to claim 1, Drabenstott et al. discloses, as claimed, a processing core (processing elements: PE1, PE2, and PE3 see Fig. 1) comprising: one or more processing pipelines having a total of N-number of processing paths (N=4 for the Drabenstott et al.'s system shown in Fig. 1), each of said processing paths for processing instructions on M-bit data words (the data can be either 32 or 64 bits, see the 32-bit data bus 126 as shown in Fig. 1, and Col. 2, line 43 regarding 64-bit data types); and a plurality of register files (PE CONFIG REGISTER FILEs, 127, see Fig. 1), each having Q-number of registers(note Drabenstott et al.'s register files (PE CONFIG REGISTER FILEs, 127, see Fig. 1) inherently comprises Q register

each), said Q-number of registers being M-bits wide; wherein said Q-number of registers within each of said plurality of register files (PE CONFIG REGISTER FILEs, 127, see Fig. 1) are either private or global registers, and wherein when a value (the data value such as in BCAST DATA BUS 126, see Col. 6, lines 34-36) is written to one of said Q-number of said registers which is a global register within one of said plurality of register files, said value is propagated to a corresponding global register in the other of said plurality of register files (since the data is broadcasted data in the BCAST DATA BUS 126, see Fig. 1), and wherein when a value (the data value exchanged between the PE register files 127 see Fig. 1) is written to one of said Q-number of said registers which is a private register (since the data value are only exchanged between the PE register files 127 see Fig. 1) within one of said plurality of register files (PE CONFIG REGISTER FILEs, 127, see Fig. 1), said value is not propagated to a corresponding register in the other of said plurality of register files. Note Drabenstott et al. also discloses the limitations of claim 17 as set forth above in claim 1.

Referring to claim 10, Drabenstott et al. discloses, as claimed, a VLIW processing core (processing elements: PE0, PE1, PE2, and PE3 see Fig. 1) comprising: one or more processing

pipelines each including a fetch stage (using I-fetch unit 103, see Fig. 1), a decode stage (inherent stage in a pipeline), an execute stage (using execution units, MAU, ALU, DSU, STORE, and LOAD see Fig. 1), and a write-back stage (inherent stage in a pipeline), said execute stage having an execute unit comprising an integer processing unit (such as MAU, or ALU see Fig. 1 when input data are integer), a load/store processing unit (such as STORE, and LOAD see Fig. 1), a floating point processing unit (such as MAU, or ALU see Fig. 1 when input data are floating point), or any combination of one or more of said integer processing units, said load/store processing units, and said floating point processing units; and a register file (PE CONFIG REGISTER FILEs, 127, see Fig. 1) for each of said one or more processing pipelines (note as shown in Fig. 1, each pipeline has one register file 127, see Fig. 1); wherein an integer processing unit and a floating point processing unit within said one or more processing pipelines both access said register file (PE CONFIG REGISTER FILEs, 127, see Fig. 1). Note Drabenstott et al. also discloses the limitations of claims 5, 15, 6, and 16 as set forth above in claim 10 wherein N-number (N=4 for the Drabenstott et al.'s system shown in Fig. 1), and M-bit data words (the data can be either 32 or 64 bits, see the 32-bit data

bus 126 as shown in Fig. 1, and Col. 2, line 43 regarding 64-bit data types) are set forth above.

Referring to claim 11, Drabenstott et al. discloses, as claimed, in a computer system, a scalable computer processing architecture, comprising: one or more processor chips (see Fig. 1), each comprising: a processing core (processing elements: PE1, PE2, and PE3 see Fig. 1), including: a processing pipeline having N-number (N=4 in Fig. 1) of processing paths, each of said processing paths for processing instructions on M-bit data word (the data can be either 32 or 64 bits, see the 32-bit data bus 126 as shown in Fig. 1, and Col. 2, line 43 regarding 64-bit data types); and one or more register files (PE CONFIG REGISTER FILEs, 127, see Fig. 1), each having Q-number of registers (note Q is a variant. Drabenstott et al.'s VLIW is inherently having Q number), said Q-number of registers being M-bits wide; an I/O link (PE local memory & data bus interface, 157, 157', 157', see Fig. 1) configured to communicate with other of said one or more processor chips or with 1/O devices (since the processor, as shown in Figs. 1 and 5B, is a VLIW-based processor, see also Col. 6, lines 12-15, regarding "SP/PE0 and the other PEs use a five instruction slot iVLIW architecture which contains a very long instruction word memory (VIM) 109"); a communication controller (cluster switch 171 see Fig. 1, and Col. 6, lines 43-

44) in electrical communication with said processing core and said I/O link (PE local memory & data bus interface, 157, 157', 157', see Fig. 1); said communication controller (cluster switch 171 see Fig. 1, and Col. 6, lines 43-44) for controlling the exchange of data between a first one (such as that comprising PE1) of said one or more processor chips (comprising processing elements: PE1, PE2, and PE3 see Fig. 1) and said other (such as that comprising PE2) of said one or more processor chips (comprising processing elements: PE1, PE2, and PE3 see Fig. 1see Fig. 1); wherein said computer processing architecture can be scaled larger by connecting together two or more of said processor chips in parallel via said 1/O links (PE local memory & data bus interface, 157, 157', 157', see Fig. 1) of said processor chips, so as to create multiple processing core (processing elements: PE1, PE2, and PE3 see Fig. 1) pipelines which share data therebetween.

As to claims 3 and 13, Drabenstott et al. also discloses: a processing instruction comprises N-number of P-bit instructions (p=32, i.e. the instructions comprise 32 bits, see Fig. 4A-4C) appended together to form a very long instruction word (VLIW) (as set forth above, since the processor, as shown in Figs. 1 and 5B, is a VLIW-based processor, see also Col. 6, lines 12-15, regarding "SP/PE0 and the other PEs use a five instruction slot

iVLIW architecture which contains a very long instruction word memory (VIM) 109"), and said N-number of processing paths process N number of P-bit instructions in parallel (note the above N, P, and M are variant. Drabenstott et al.'s VLIW is inherently having N, P, and M bit number).

As to claims 8 and 19, Drabenstott et al. also discloses: each of said plurality of register files (PE CONFIG REGISTER FILEs, 127, see Fig. 1) is connected to a bus (BCAST DATA BUS 126, see Col. 6, lines 34-36), and a value written to a global register in one of said plurality of register files is propagated to a corresponding global register in the other of said plurality of register files across said bus.

As to claims 9 and 20, Drabenstott et al. also discloses: said plurality of register files (PE CONFIG REGISTER FILEs, 127, see Fig. 1) are connected together in serial, and a value written to a first global register in a first of said plurality of register files is propagated to a corresponding first global register (note the number of the register could be broadly defined since it was not well defined previously) in a second of said plurality of register files connected directly to said first of said plurality of register files (PE CONFIG REGISTER FILEs, 127, see Fig. 1).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drabenstott et al. in view of Masubuchi (USP 5,530,817), hereafter referred to as Masubuchi'817.

Drabenstott et al. discloses the claimed invention except for: every two of said N number of processing paths share one of said plurality of register files.

Masubuchi'817 discloses a VLIW computer comprising: every two of said N number of processing paths (for ALUs 13 and 14, se Fig. 1) share one (register file 12, see Fig. 1) of said plurality of register files (register files 12 and 22, see Fig. 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Drabenstott et al.'s system to comprise every two of said N number of processing paths share one of said plurality of register files, as taught by Masubuchi'817, in order to reduce the number of register files in the Drabenstott et al.'s system.

14. Claims 4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drabenstott et al.

Drabenstott et al. discloses the claimed invention comprising N=4, M=64, and P=32, as set forth above, except for explicitly showing: using Q=64 registers in the register file.

However, it is well known in the art to have a computer system having Q=64 registers in the register file.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Drabenstott et al.'s system to comprise having Q=64 registers in the register file since it is just an alternative bit size comparing with that used in the Drabenstott et al.'s system.

Further, as shown in re Rose, 105 USPQ 237 (CCPA 1955), to make changes in size/range generally does not provide patentable weight to the claimed invention.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, wherein Levy et al.'175 also discloses private and global registers in register file as the claimed invention; Pechannek et al.'776 and Pechannek et al.'356, discloses the processing elements in a highly parallel processing system; and Pechannek et al.'753 discloses the switch used in the I/O link for the communication of processing elements.

Contact Information

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2100 receptionist whose telephone number is (703) 305-3900.

17. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into the Group at fax number: 703-872-9306. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

April 21, 2004